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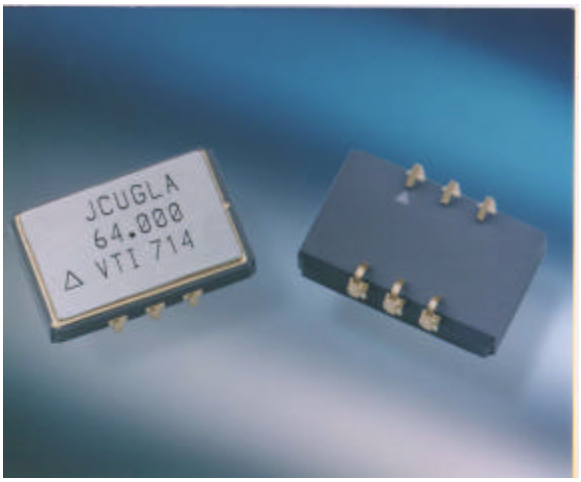
Product Data Sheet

J-Type
Voltage Controlled Crystal Oscillator



The J-Type Voltage Controlled Crystal Oscillator

Features

- Industry Standard 6 Pin J-Lead Ceramic SMD
- Small 14mm X 9mm Package
- Advanced Custom ASIC Technology
- Absolute Pull Range Performance beyond 100 ppm
- Available Output Frequencies to 155.52 MHz
- 3.3 Volt or 5.0 Volt Supply
- CMOS or TTL Output with Tri-State
- Low Phase Noise Versions Available
- Commercial or Industrial Temperature Range
- EIA Compatible Tape and Reel Packaging

Description

The J-Type Voltage Controlled Crystal Oscillator expands VTI's advanced VCXO performance capabilities while adhering to a package footprint compatible with the industry-common J-Lead package.

Performance advantages include superior phase noise, improved linearity, higher frequencies, tighter stability and increased pull. Advanced custom ASIC technology results in a highly robust, reliable and predictable device.

The J-Type VCXO is a quartz stabilized square-wave generator capable of driving either a CMOS or TTL load. The device is packaged in a 6 pin J-Lead ceramic package with a seam welded lid.

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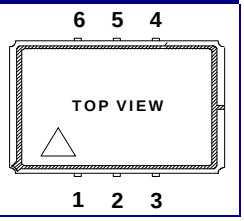
Pin Information

Table 1. Pin Function

Pin	Symbol	Function
1	V_C	VCXO Control Voltage
2 (5)[1]	N.C.	No User Connection
3	GND	Case Ground
4	Output	VCXO Output
5 (2)[1]	Tri-State	TTL Low to Disable Output. TTL High or Float to Enable Output.
6	V_{DD}	Power Supply Voltage (3.0 V ±10%, 3.3 V ±10% or 5.0 V ±10%)



1. Alternate pin configuration for tri-state control on pin2. Alternate configuration is indicated by the last letter of the code "D" as indicated in table 6.

Performance Characteristics

Table 2. Electrical Performance

Parameter	Symbol	Minimum	Typical	Maximum	Units
Supply Voltage[1]	V_{DD}	0.9* V_{DD}	V_{DD}	1.1* V_{DD}	V
Supply Current	I_{DD}	10 mA + 0.25 mA/MHz Typical			mA
Output Voltage Levels[2]					
Output High	V_{OH}	0.8*V_{DD}			V
Output Low	V_{OL}			0.1* V_{DD}	V
Transition times[2]					
Rise Time	T_R			5.0	ns
Fall Time	T_F			5.0	ns
Duty Cycle[3]	D	45	50	55	%
Nominal Output Frequency[4]	f_0	183E-6		155.52	MHz
Absolute Pull Range	APR	See Part Numbering and APR Section			ppm
Control Voltage	V_C	0		V_{DD}	V
Center Voltage	V_0	Please Contact VTI for Details			V
Leakage Current of Control Input	I_C	-1		1	µA
Control Voltage Bandwidth (-3 dB, V_C=0.5*V_{DD})[5]	BW		10		kHz
Gain Slope @ V_0	$\Delta f/\Delta V_C$		150		ppm/V
Phase Noise	ϕ_N	Contact VTI for Phase Noise Specifications			dBc/Hz

1. A 0.1 µF low frequency tantalum bypass capacitor in parallel with a 0.01 µF high frequency ceramic capacitor is recommended.
2. Figure 1 defines these parameters. Figure 2 illustrates the equivalent 5-gate TTL load and operating conditions under which these parameters are specified and tested.
3. Duty cycle is defined as (on time÷period), with V_S = 1.4 for TTL or V_S = 2.5 V for CMOS, per Figure 1.
4. Other frequencies may be available, please contact factory with your special requirements.
5. Wider bandwidth versions are available, please contact VTI for details.

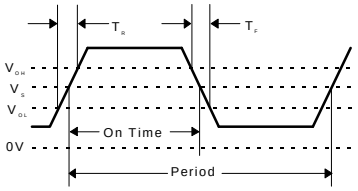


Figure 1. Output Waveform

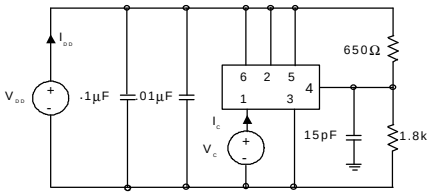


Figure 2. Output Test Conditions (25±5°C)

Absolute Pull Range (APR) Specification

The frequency deviation of the J-Type VCXO is specified in terms of Absolute Pull Range (APR). APR provides the user with a guaranteed specification for minimum available frequency deviation over all operating conditions. Operating conditions include operating temperature range, power supply variation, differences in output loading and changes due to aging.

A J-Type VCXO with an APR of +/-50 ppm will track a +/-50 ppm reference source over all operating conditions. The same device will typically demonstrate a Total Pull capability of 150 to 350 ppm. Absolute Pull Range (APR) is specified by the fourth character of the product code in Table 6. *Please contact VTI for the APR Application Note.*

Oscillator Aging

Quartz stabilized oscillators typically exhibit a small shift in output frequency during aging. The major factors which lead to this shift are changes in the mechanical stress on the crystal and mass-loading of foreign material on the crystal.

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As the oscillator ages, relaxation of the crystal mounting stress or transfer of environmental stress through the package to the crystal mounting arrangement can lead to frequency variations. VTI has minimized these two effects through the use of a miniature AT-Cut strip resonator crystal which allows a superior mounting arrangement and results in minimal relaxation and almost negligible environmental stress transfer.

Mass-loading on the crystal generally results in a frequency decrease and is typically due to out-gassing of material within a hermetic package or from contamination by external material in a less than hermetic package. VTI has minimized the impact of mass loading by ensuring hermetic integrity and minimizing out-gassing by limiting the number of internal components through the use of ASIC technology.

Under normal operating conditions with an operating temperature of 40°C, the J-Type will typically exhibit 2 ppm aging in the first year of operation. The device will then typically exhibit 1 ppm aging the following year with a logarithmic decline each year thereafter.

Handling Precautions

Although protection circuitry has been designed into this device, proper precautions should be taken to avoid exposure to electrostatic discharge (ESD) during handling and mounting. VTI employs a human-body model (HBM) and a charged-device model (CDM) for ESD-susceptibility testing and protection design evaluation.

ESD voltage thresholds are dependent on the circuit parameters used to define the mode. Although no industry-wide standard has been adopted for the CDM, a standard HBM (resistance = 1500Ω, capacitance = 100pF) is widely used and therefore can be used for comparison purposes. The HBM ESD threshold presented here was obtained by using these circuit parameters.

Table 3. ESD Threshold Voltage

Model	Threshold	Unit
Human-Body (HBM)	1500*	Volts Min.
Charged-Device (CDM)	1500	Volts Min.

*Mil-STD-883D, Method 3015, Class 1

Table 4. Environmental Compliance

Parameter	Conditions
Shock and Vibration	MIL-STD-883C, 2002.3 A, 2007.1 A
Mechanical Vibration	MIL-STD-883C, 2007.1 A
Lead Solderability	MIL-STD-883C, 2003.5
Fine and Gross Leak	MIL-STD-883C, 1014.7
Storage Temp.	-55°C to 125°C

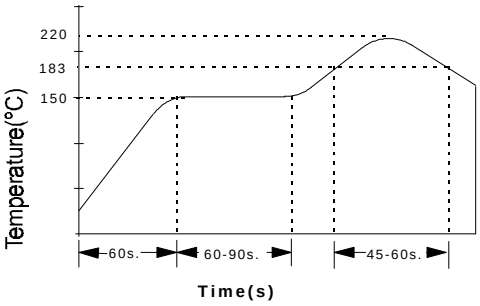

Figure 3. Suggested Reflow Profile

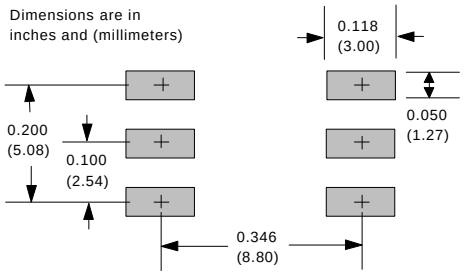

Figure 4. Suggested Pad Layout

Tape and Reel Information

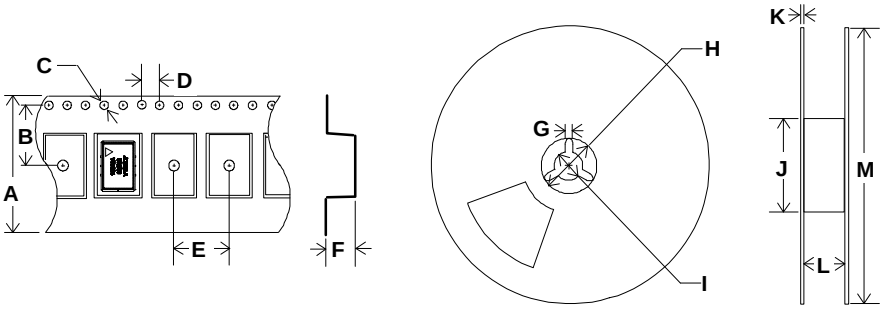

Figure 5. Tape and Reel Information

Table 5. Tape and Reel Dimensions (Dimensions are in mm)

A	B	C	D	E	F	G	H	I	J	K	L	M
24.0	11.51	1.5	3.99	11.99	4.8	1.78	20.6	13.0	63	5.0	25	330

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Outline Diagram

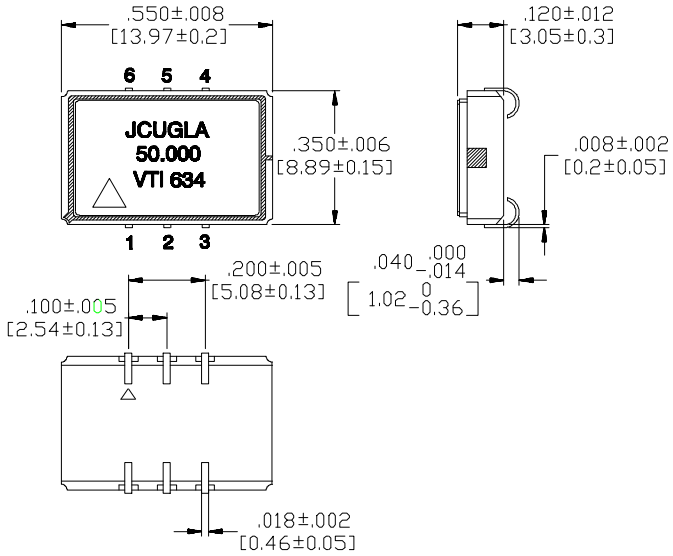

Figure 6. Outline Diagram

Ordering Information

Table 6. Part Numbering

Example Part #	J	C	U	G	L	A
	Package	Supply Voltage (V)	VCXO Type	APR (ppm)	Operating Temp. (°C)	Output Symmetry
	J 6 J-Lead Ceramic	C 5.0±10%	U Standard	C ±20	C 0 to 70	A TTL 50±5% pin 5 TriState
		D 3.3±10%	L 10% Linearity	F ±32	L -40 to 85	J CMOS 50±5% pin 5 TriState
			M ±20 ppm Stability	G ±50		D CMOS 50±5% pin 2 TriState
				N ±80		
				H ±100		

Note: Not all combinations are feasible, please contact VTI for details

Standard Frequencies (MHz)						
13.000	16.384	19.440	19.6608	20.480	24.704	26.000
27.300	32.768	34.368	37.056	38.880	40.960	44.736
49.152	51.840	62.208	64.000	65.536	77.760	155.520

Note: Other frequencies are available upon request, please contact VTI for details